

# PARASITIC CAPACITANCE–PREVENTING DUMMY SOLDER BUMP STRUCTURE AND METHOD OF MAKING THE SAME

## Abstract

A parasitic capacitance–preventing dummy solder bump structure on a substrate has at least one conductive layer formed on the substrate, a dielectric layer employed to cover the conductive layer, an under bump metallurgy layer (UBM layer) formed on the dielectric layer, and a solder bump formed on the UBM layer.